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COMMON SYSTEMS

MAIN STORE CONTROLLER AND MEMORY
CIRCUIT

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SECTION I - GENERAL DESCRIPTION1. PURPOSE OF CIRCUIT

1.01 The main store controller and memory (MASC) circuit contains the main store controller (MASC) circuit which is the interface between the 3A central control (3A CC) and main store memory (MASM) circuits. The MASC contains one or two main store memory modules. The MASC performs the following functions:

- Controls the storage and retrieval of data to and from the MASM in response to commands from the 3A CC
- Controls the refreshing of data in the memory modules
- Performs error checking
- Collects diagnostic and error information to be sent to the 3A CC.

2. GENERAL DESCRIPTION OF OPERATION

GENERAL OPERATION

2.01 Normal communications between the 3A CC and MASC occur over the parallel main store bus (MASB), while diagnostic-access and error-definition transfers occur over a serial I/O subchannel (IOSC). The MASB carries address, data, control, and command information from the 3A CC to the MASC; and data, control, and error flag information from the MASC to the 3A CC. The main store (MAS) operates asynchronously with respect to the 3A CC, ie, an MAS operation is initiated by a 3A CC command, but no other timing synchronism is required for completion of the operation.

2.02 Commands are received by the MASC over the MASB, and decoded and executed by the MASC and the MASM. Address information is received over the MASB, registered by the MASC, and passed on in appropriate form to the fanout boards (FOBS) of the MASM. Data-word bits are received (for a write operation) or transmitted (for a read operation) over the MASB, and a data parity check is performed for either a read or write operation.

2.03 The MASC controls the refreshing of MASM data. The clock is counted down, and approximately every 34.3 USEC appropriate control signals are issued to the memory modules to effect the accessing of one row on every memory chip in the MAS simultaneously. Since reading data from a row of memory cells also rewrites data back into the cells, the data is refreshed. The MASC also contains refresh address sequencing circuits which insure that every location in the MAS is refreshed at least once every 4.4 ms, thus insuring data integrity.

2.04 Since the MAS operates asynchronously with respect to the 3A CC, the MASC generates its own internal check and timing signals. The timing circuitry sets up the

proper sequencing for internal information transfers, control signals to the MASH, and error-detection checks. The time states are under the control of a crystal clock and a shift register.

2.05 The MAS performs a number of error checks during normal operations. In addition to the data parity check already mentioned, checks are made on such internal MASC functions as timing sequences, register loading, refresh timing, MASH states, and write-protect status. The write-protect circuitry insures that certain write-protected areas of memory are not unintentionally altered. Additionally, there are MASC check circuits which collect diagnostic information from the FOBs of the MASH pertaining to proper memory module selection, control signal occurrences, and address parity. This information is distilled by the MASC and passed on to the 3A CC when necessary.

2.06 As a periodic maintenance operation, or as a response to error signals from the MASC check circuitry, the 3A CC may perform diagnostic operations on the MAS. Diagnostic communications between the 3A CC and MASC occur over the IOSC. The MASC receives and decodes diagnostic commands which can access the MAS circuitry. Error-status information can be transmitted back to the 3A CC, which can analyze the error information and take appropriate corrective action.

2.07 The MASH contains, in addition to control circuitry, one or two memory modules. This memory represents either 128K or 256K (K=1024) words of storage. The word length is either 18 bits or 26 bits.

2.08 The MASH contains power supplies for its memory module(s) and logic circuit packs. In conjunction with this, it contains power sequencing circuits to insure that the supplies are activated in the correct sequence, and power initialization circuits to preset certain control circuits to their proper initial states.

EQUIPMENT ARRANGEMENT

2.09 The MASH is made up of two apparatus-mounting levels. The control circuitry and associated power supplies occupy the upper level, and the memory module(s) and associated power circuits are housed in the lower level.

SECTION II - DETAILED DESCRIPTION

1. CONTROL AND TIMING (FS 1)

1.01 The major control of the main store and the principal communication control link between the main store and the 3A CC is contained in FS 1. Although the control and timing element is spread over many circuit packs (CPs) the large majority of the element is contained on the FA1071.

FA1065, and FA1068 CPs, with the FA1071 CP being the greater part of FS 1 from the standpoint of cycle control. Composite diagram 1 shows an overall block diagram of the principal segments of the element. In general, FS 1 contains the following subcomponents:

- (a) Crystal controlled clock
- (b) Timing shift register
- (c) Cycle control components, ie, flip-flops
- (d) Command register and decoding
- (e) Main store bus receiver and repeaters for control signals
- (f) Complement correction circuitry
- (g) Main store selection circuitry.

1.02 The control and timing element of the main store supplies, throughout the system, the necessary timing and control to execute a main store cycle and the self-checking circuitry features of the main store. The internal functions, once a cycle is initiated, are sequenced with the main store's own internal clock. The clock is a 14.925373-MHz crystal oscillator located on the FC203 CP. FS 1, in addition to managing a main store cycle generated by the 3A CC, also controls the sequence of operation entailed in performing a refresh cycle.

1.03 The inputs from the 3A CC, excluding address and data, that control the main store cycle are the four command bits and store go. All signals that are generated within the main store or returned to the 3A CC emanate from an active signal on store go (SGO). Two other inputs from the 3A CC, complement write and automatic correction, are used in an error correction scheme and are discussed later.

1.04 Within FS 1, symbol 1, is a 14-bit shift register which provides all the timing for control of a 3A CC initiated command or a refresh cycle. This timing shift register is normally inactive and is activated by a command for a main store cycle by the 3A CC or an internal request from the main store to perform a refresh cycle. The timing shift register produces every 67 nanoseconds for a total time of 938 nanoseconds. Shifting a single active bit through the timing shift register is accomplished by the crystal-controlled clock in the main store. The timing shift register is started when the SGO lead from the 3A CC goes active. Since the 3A CC and the main store crystal clock are not synchronized, a period of from 0 to 67 nanoseconds will elapse from the time input SGO10 goes active until the first edge of the main store clock that causes a shift into the first bit of the timing shift register. The fact that the 3A CC

must wait for the proper phase of the main store clock is part of the asynchronous nature of the communications between the main store and the 3A CC.

1.05 The interconnection of main stores when a processor complex contains more than one main store is accomplished by receiving all bus signals from the 3A CC in each main store and repeating them to higher-order main stores. This bus receiver and bus repeater arrangement is also used for returning signals to the 3A CC, where each main store receives the bus signals from higher-order main stores and repeats them to lower-order main stores or the 3A CC. In order to meet the main store bus requirement for relative timing of bus signals, three bus signals pass through delay lines in the main store. SGO10 is delayed before being repeated to a higher-order main store. Store complete (SCM10) and store error C (SERC10) are delayed before being repeated to lower-order main stores. The delay lines are located on the PC262 CP. In a processor containing only one main store on the bus, none of the repeater circuitry or delay lines is used, since the function of these is only concerned with systems having multiple main stores.

1.06 Four command bits are sent by the 3A CC with each cycle in a 2-out-of-4 code. This code designates the type of main store cycle that is to be performed, ie, read or write, and appropriately sets up the conditions necessary for a particular cycle. The following is a list of the command codes and their functions:

COMMAND CODE BITS				FUNCTION
SC3	SC2	SC1	SC0	
0	0	1	1	WRITE
1	1	0	0	READ
0	1	1	0	STORE WRITE PROTECT INFORMATION IN MAIN STORE
1	0	0	1	READ WRITE PROTECT INFORMATION FROM MAIN STORE
0	1	0	1	BLIND WRITE*
1	0	1	0	SPARE READ+

* Blind write code can only be used when accompanied by a wiring option on the main store controller backplane.

+ Spare read is a nonusable code; while it is decoded in the main store it is not presently used in an assigned function.

1.07 Composite diagram 2 is a more expanded view of FS 1, showing many internal gates and flip-flops from the FA1071 CP. All parts on this composite not specifically labeled are located on FA1071.

1.08 The first activity to occur in the main store when a cycle is requested is to load address, data, and command information from the bus. Loading information from the main store bus starts when SGO10 goes active, producing an active

signal on output normal load. The signal, normal load, is terminated when flip-flop SBY is set. The contents of the main store bus is loaded into the main store in a clear and gate operation by the signal on the normal load net. The clear and gate operation requires a normal load signal and its complement; the leading edge of the normal load pulse clears the respective register and the trailing edge will lock the new information into the register. In a system containing more than one main store, each main store on the bus will internally generate a normal load signal and gate the information from the main store bus. Only the main store, which decodes address bits 18 and 19 indicating "this" store, will execute a cycle. Other main stores on the bus will terminate execution of the cycle.

1.09 An additional consideration for the main store is the direction of the bus. Since the data bus to the main store is bidirectional, the 2-out-of-4 bit command code must be interpreted to indicate if the bus should be pointing toward the main store in the case of a write command or pointing towards the 3A CC in the case of a read command. Store command bit 3 is set up in the 2-out-of-4 code to be a 1 when a main store read is to be executed. Store command bit 3 being active will set the bidirectional data repeaters to point toward the 3A CC. Composite diagram 3 shows the bus receiver and repeaters used in the main store. Even though not all of the bus repeaters are contained in FS 1, they are shown here for completeness.

1.10 The control of the main store cycle, both normal and refresh, is shown in composite diagram 4. A main store cycle is started by loading an active bit into shift register SHB00 and shifting it through the shift register by the main store clock (CLOCK0A). The following is a functional description of the control flip-flops associated with the timing shift register.

IDLE - This flip-flop is set any time there is not an active bit in the shift register. The output of each individual bit in the shift register is ANDed together and, if all stages are inactive, the idle flip-flop is set. The idle flip-flop is cleared when an active bit is loaded into the first stage of SHB00.

SBY - The store busy flip-flop is set when shifter bit SHB02 is active and the main store is selected and not in a refresh mode. SBY is only set when the 3A CC generates a refresh cycle; it is not set during a refresh cycle. The SBY flip-flop is cleared when SGO goes inactive on the main store bus and the idle or the mode flip-flops are set.

MODE - This flip-flop, when set during a cycle, indicates that a refresh

cycle is in operation, in contrast to a cycle generated by an active signal on the main store bus. The mode flip-flop is cleared at shifter bit 12 time, shifter stage SHB12 active.

FRQ - This flip-flop from FS 3 is set anytime the main store requests a refresh cycle.

1.11 A normal main store cycle is started when bus signal SGO goes active. Gate TLSHQA0 will load an active bit into the first stage under the following conditions.

- (a) SGO active.
- (b) Idle flip-flop is set (no active bit in the shift register).
- (c) SBY flip-flop is cleared.
- (d) The refresh request (RREQ) flip-flop from FS 3 is not set.

1.12 As soon as an active bit is loaded into the first stage of the shift register by gate TLSHQA0, the idle flip-flop is cleared and no further bits can be loaded into the shift register until both the idle and the SBY flip-flops are returned to their inactive states. A refresh cycle is started in a similar manner as a normal cycle by also loading a bit into the first stage of the shift register. In the case of a refresh cycle, the cycle is initiated when the RREQ flip-flop is set and gate TLSHQA0 loads a single bit into the first stage of the shift register. When the RREQ flip-flop is set, if the idle flip-flop is also set, the mode flip-flop will be set. Output states from the mode flip-flop will be the signals used throughout the main store that control the variation between a refresh and a normal cycle. The mode flip-flop is reset when shifter bit SHB12 goes active.

1.13 Composite diagram 5 of FS 1 shows the four command bits from the 3A CC. The command bits are in a 2-out-of-4 bit code and are loaded from the bus by the normal load signal. The command bits are also repeated to higher-order main stores. Information from the bus is put into registers C0 through C3. The outputs from the command code registers are decoded to the six states that determine the particular type of main store cycle and are distributed in the main store for controlling or enabling that function. The four command code registers are cleared at the end of each cycle when SGO and SBY are inactive.

1.14 Only two of the six decoded commands will result in a write taking place in the memory. These commands, write and blind write, will force outputs RWQA and RWOB active (write state). A decoded state other than write and blind write will force outputs RWQA and RWOB inactive (read state). In addition, a write protect

violation or a refresh cycle will force outputs RWQA and RWOB inactive. Output NOCS0 is a net that when active will force the chip select signal to the inactive state. This net is active when the command code indicates a main store cycle other than one that requires memory access. The main store cycles that do not cause memory access are spare read, read the write protect registers, and write the write protect registers. A refresh cycle will force net NOCS0 inactive since a chip select signal is always required during refresh.

1.15 Address bits 18 and 19 on the main store bus are used to designate the particular main store that is to respond to a memory cycle initiation. Each main store connected to the bus is wired on the main store controller backplane to reflect the decoding of address bits 18 and 19. The wiring connection and decoding are shown on composite diagram 6. The main store decoding is duplicated on two CPs, FA1071 and FA1062, for error checking. The actual decoding takes place on FA1071 and the main store decoding on FA1062 serves as a check of the decoding circuitry. A discrepancy between the decoding on the two CPs will set the SEL side of the SEL.SHER flip-flop and will cause error A on the main store bus.

1.16 Composite diagram 7 is an idealized timing chart of the relative timing of the major control signals and does not reflect any gate delays that would be present in the actual appearance of signals. SGO and the main store crystal clock (CLK) can be in any position in relationship to each other. The appearance of signal SHB00, the output from the first bit in the timing shift register, will depend on whether SGO is active when the CLK phase is in a position to load a bit into the shift register, which is an edge-triggered delay flip-flop. As noted on the timing diagram, the signals R/W, SBY, SCM, and error C are reset by a combination of conditions. A new main store cycle can be started if SGO and SCM or error C are inactive on the main store bus.

2. ADDRESS AND DATA (FS 2)

2.01 The main store address register is a group of 22 registers physically distributed in a bit slice manner, as shown in composite diagram 1.

2.02 The address is loaded from the bus by the normal load signal developed in FS 1. Each of the address bits is loaded simultaneously from the main store bus when the bus signal SGO goes active. In addition to accessing the address register in memory, outputs of the address register are used in FS 4 to decode register locations used in the main store write protect scheme.

2.03 Driving the memory from the address registers is done in two branches, A and B. Each of the address register stages

has two high-power gates on the output of the respective circuit boards to drive the memory. The A branch is configured to drive memory module 0, and the B branch drives memory module 1.

2.04 Address bits 18 and 19, used to define the actual main store on the bus that responds to a command, are not sent to the memory since they do not define an actual memory location within a main store. Since address parity high on the bus is calculated using address bits 18 and 19, the parity high bit in the main store must be recalculated to remove the influence of address bits 18 and 19 before being sent to the memory. The actual parity test for the address is done in memory FS 7. Address parity low is sent directly to memory for verification of correct address parity. The address parity low bit is calculated over address bits 0 through 7 and the address parity high bit is calculated over address bits 8 through 19.

2.05 A typical stage of an address register is shown in composite diagram 2. The composite represents an address register stage on an FA1060 CP that also has a refresh address counter stage multiplexed to the memory drivers. Address register stages that are not located on an FA1060 CP do not contain a stage of refresh address counter. In addition, not all refresh address registers on the FA1060 CPs are used as part of the refresh address counter. A further discussion of the refresh address register appears in FS 3.

2.06 The address is loaded from the main store bus by the normal load (NLD0) signal in a clear and gate manner and repeated to higher order stores. When the main store is not in a refresh mode, the address register output goes directly to the memory via A and B branch drivers. In a refresh mode, the address to the memory is taken from the refresh address register and not from the normal address register. All address bits to the memory are connected via the fanout boards.

2.07 Additional information on composite diagram 3 shows that the contents of the address register can be returned via the data bus for diagnostic purposes. This is covered in FS 5.

2.08 The data registers have a physical layout similar to the address registers. The data bits are bit-sliced and are located in the positions shown in composite diagram 3. Note the FA1060 CPs that are removed for an 18-bit-wide data word (16 data and 2 parity). For a 26-bit-wide data word (24 data and 2 parity) all CPs are inserted. The FA1067 CP, which performs 3-bit to 2-bit parity conversion for a 26-bit-wide main store, is also removed when the data word is 18 bits wide. The signal flow of the data bits is shown in composite diagram 3. The signal flow is drawn to represent a write cycle where data from the bus is being loaded into memory.

Along with actual data paths connecting the data registers to the memory is the parity check circuitry involved in testing the validity of the data word.

2.09 Symbol No. 18 contains the circuitry for conversion of the 3-parity bits received on the main store bus to the 2-parity bits that are stored in memory. For main stores using an 18-bit word the inputs to the PH and PL data registers are taken directly from the main store bus. In a full size main store, data bits 16 through 19 are combined with the parity low bit, input NO2DPH10, to form a new parity low which is stored in memory. Likewise, data bits 20 through 23 are combined with the parity high bit, input NO2DPH10, to form a new parity high which is stored in memory. The remaining parity bit on the bus, SDEPH10, originally the parity over data bits 16 through 23, is tested against the calculations of parity over the same data bits in the main store. A discrepancy between them will cause a bit to be set in the error register. A further explanation of the circuitry involved in the data parity of a 26-bit store is covered in composite diagram 6.

2.10 The flow of data from the main store controller to the memory planes is shown for data bits 0 and 8, and parity bits PL and PH. For illustrative purposes only these four write data lines are shown, because of the large number of leads. All signals that go between the controller and the memory planes are buffered by the fanout boards except the write and read data lines, which are connected directly to the data registers in the controller to the memory planes. Like the address connections to the fanout boards, the read and write data lines are driven in an A and B branch, with the A-branch going to memory module 0 and the B-branch going to memory module 1.

2.11 Each of the data registers have an additional output which connects to FS 5 (error detection). Composite diagram 3 illustrates the signal flow during a memory write. If the parity check fails, an error bit is set in the error register. Two separate stages of the error register are dedicated to the data parity check during memory writes. One of the error register bits captures any errors in the parity check over the data parity high field and the other captures errors over the data parity low field.

2.12 Composite diagram 4 shows the information flow of the data, but, as indicated by the arrows, this is the direction of data flow for a memory read cycle. Again, only data bits 0 and 8 (parity low and parity high) are shown, due to the large number of leads that would be required for all the data bits. As in a write cycle, the parity bits must be recalculated to form three data fields from the memory, which has the parity calculated over two data fields. The parity bits are recalculated into the original three data

fields by the circuitry in symbol 18 and returned on the main store bus in the same form as received during a write cycle.

2.13 The results of the data parity test during a main store read cycle are used differently than those of a write cycle. The normal response during a write or read cycle that does not have a data parity failure is to return a store complete signal (SCW00) on the main store bus. If a parity failure occurs during a read cycle either from the parity high data field or the parity low data field or both, an error C SERCO0 signal is put on the main store bus in place of the store complete signal. A discussion of read parity failures is covered in FS 5.

2.14 Composite diagram 5 shows a single stage of the data register. The bit slice layout of the main store has two such data registers on each bit slice CP that composes the full data register. Each of the data register stages can be loaded from the main store bus (write) or from the main store memory (read). The following is a list of the principal control and data signals into and out of the data register, along with their functions.

<u>NET NAME</u>	<u>FUNCTION</u>
COMWRT0A	Complement write for error correction. Complements data to the memory during a complement write cycle.
NLD0	Normal load signal that gates data from the main store bus into the data registers.
SD0010	Data to or from the main store bus.
DSTB0	Data strobe, used to load the data registers from the memory during a read cycle.
RD000A RD000B	Data from the memory A and B branches.
COMPRD0A	Complement read for error correction. Complements data from the data register before being put on the main store bus during an error correction read cycle.
ASELO	Main store select signal derived from address bits 18 and 19. When this main store is selected (ASELO = active), the data contained in the data register is put on the main store bus. When the ASELO signal is inactive, the main store bus from higher-order main stores is enabled.
BUSRD0A	Bus read is a signal derived from the command code and sets the main store data bus either in the direction away from the

3A CC (write) or towards the 3A CC (read).

2.15 As mentioned earlier, a main store with an 18-bit wide word (16 data, 2 parity) has the 2-parity bits loaded directly into the data register from either the memory or the main store bus. In the case of a main store with a 27-bit wide word (24 data, 3 parity) the 3-parity must be recalculated to form 2-parity bits over the data word before being stored in memory. Likewise the 2-parity bits in memory must be recalculated to form 3-parity bits over the data word before being returned on the main store bus. Composite diagram 7 shows the essence of the circuitry involved in the manipulation of the parity bits.

2.16 The data received by the main store consist of three data fields of eight bits and three parity bits that are calculated over each of the three data fields. The resultant 2-parity bits that are put into memory are derived by breaking the upper data field, bits 16 through 23, into two parts, bits 16 through 19 and 20 through 23. The calculated parity over data bits 16 through 19 is combined with the data parity low bit from the main store bus to form a new data parity low that represents parity over a 12-bit data field. In the same manner, the calculated parity over data bits 20 through 23 is combined with the data parity high bit to form the second parity bit that is calculated over the remaining 12 bits of data.

2.17 Referring to composite diagram 6, exclusive OR gates are used to show the conversion of parity states from 8-bit to 12-bit fields and the reverse 12-bit to 8-bit fields. During a main store write cycle the calculated parity over data bits 16 through 19 is combined with the data parity low bit by gate A. The result on the output of gate A is loaded into the parity low data register, where its contents are used to write into the memory. The same combination using data bits 20 through 23 and parity high is accomplished by gate B, with the result loaded into the parity high data register. Also during a write cycle the resultant parity from data bits 16 through 19 and data bits 20 through 23 are combined by gate F. The output of gate F is combined with the extended data parity high bit from the main store bus. The output of gate G tests whether the parity was properly generated over the two 4-bit fields and agrees with the extended parity high bit on the bus. A failure to properly calculate parity during a write cycle will cause a bit to be set in the main store error register.

2.18 The reverse situation occurs in composite diagram 6 during a read cycle. Gate C strips the parity calculated over data bits 16 through 19 from the contents of the parity low data register which contains the parity read from memory. The output of gate C will now contain the parity over the original 8-bit data field

that was received by the main store. Gate D performs the same operation for data parity high. To return the parity over the highest 8-bit field, gate E combines the outputs of the two parity trees and returns on the main store bus the recreated extended parity high bit.

3. REFRESH CONTROL (FS 3)

3.01 The main store memory, being a dynamic random access memory, requires that the memory be refreshed or rewritten on a periodic basis. A refresh cycle resembles a memory read, except that a refresh cycle is internally generated and executed in the main store without a stimulus from outside the main store. The configuration within the actual memory device is such that when a read or refresh cycle is performed, an entire row of the device is rewritten to its original data content. Since the memory device is configured in a 128-row by 128-column matrix, a single memory read or refresh within a row will refresh the entire row. With 128 rows in a device, 128 cycles will refresh the entire device. During a refresh cycle all memory devices in the main store are accessed. Consequently, 1/128 of the main store is refreshed, and 128 cycles are required to refresh the entire main store. A read cycle, in contrast, does not access every device, but only those selected corresponding to the address on the main store bus. Basic requirements of the memory device require that all rows of the device be refreshed approximately every 4.4 milliseconds. The 4.4-millisecond requirement is a function of temperature and takes into account the worst case temperature rise in the main store.

3.02 The initiation of a refresh cycle is obtained by counting down the main store crystal clock by 512 to produce a refresh request (RREQ) every 34.3 microseconds. With 128 rows to be refreshed on each memory device, the entire main store is refreshed every 4.39 milliseconds. Composite diagram 1 is a complete overview of the refresh circuitry. The main store clock is counted down by the RREQ counter on CP FA1066. The counter is nine stages, shown as symbol No. 1. The output of the counter, net ARTIM1, will set the RREQ flip-flop on CP FA1071, and, when the main store is idle, a refresh cycle will be run.

3.03 An additional 9-stage counter located on the FA1062 CP, symbol No. 2, is used as a check of the active RREQ counter on FA1066. A check circuit in FS 5 tests that when a refresh cycle takes place, the duplicate RREQ counter also indicates time for a refresh.

3.04 The output from the FA1071 CP, symbol No. 3, initiates the necessary control signals to execute and monitor the refresh cycle. During the refresh cycle the refresh address is selected, symbol No. 4 through 13, as the input to the

memory. The memory in turn tests the address parity of the refresh address to determine if the refresh address register is functioning properly.

3.05 The actual interconnection of the individual stages of the refresh address register is shown in composite diagram 2. Each FA1060 CP contains two stages of the refresh address register. The outputs of each of these refreshed address register stages are multiplexed with the corresponding main store address register stage, and the generated refresh signal in the main store will select one of the two to address the memory. While each stage of refresh address is connected to a main store address register stage, the binary weight of the individual refresh addresses does not correspond to the bit position; i.e., the refresh address stage connected to the address bit 0 lines to the memory is not necessarily the least significant digit. Each refresh address register stage has an individual input and output allowing them to be interconnected in any manner. The two stages of refresh address on each FA1060 CP are labeled RAD0 and RAD1. The full interconnection of these stages is shown on composite diagram 2.

3.06 Seven stages of refresh address are required to fully refresh the main store, 128 rows on each memory device. To provide a self-checking feature for the refresh address register, it is fully duplicated in two 7-stage counters. A failure in either one of the counters will be detected as an address parity failure on the fanout board. In actual operation, only the seven address bits in the refresh address register are of importance, since they control the row address of the memory device. A full refresh address register, seven stages of read and seven stages of duplicated, is less than the number of stages that are available on all the FA1060 CP boards. Therefore, not all refresh address stages are used, and the ones not used have no interconnection as part of the counter. Those stages that are not used will always remain in a steady state. In operation, the two 7-bit refresh address registers, real and duplicated, are incremented at the end of each refresh cycle.

3.07 The refresh operation in the main store involves interweaving refresh cycles between normal store cycles, a sort of cycle-stealing operation. The interval in which the main store refresh cycles occur is determined internally by the crystal controlled clock. The clock, running at 14.9 MHz, is divided using a binary counter to produce an output every 512 clock cycles, or an output every 34.3 microseconds. Composite diagram 3 shows the circuitry for producing the refresh interval. Like the refresh address, the divide-by-512-counter is completely duplicated as a self-checking feature of the main store.

3.08 The output of the main refresh counter, symbol 1, will set the RREQ flip-flop in symbol 3 each time a refresh cycle is to be run. When the main store timing shift register in FS 1 is idle, a refresh cycle is initiated.

3.09 The output of the duplicate RREQ counter is used in FS 5 to insure that a malfunction in either counter is detected.

4. WRITE PROTECT (FS 4)

4.01 The write protect circuitry in the main store allows any 4096 words of memory to be considered as read only. Write protect is implemented with a 64-bit register, each bit in the register representing 4096 words of memory. The contents of the write protect register can be written into via the main store data bus and the contents can be read out of the register via the data bus. During each main store memory write, the contents of the write protect register is interrogated to determine if the memory location had been previously designated as a write protected area of memory. The result of a write protect violation, an attempt to write in a write-protected area, will cause the write command to be canceled, and an error bit B to be returned on the main store bus.

4.02 Composite diagram 1 is an overall view of the write protect FS. The actual write protect register is shown to contain 72 bits, which is divided into 64 write protect bits and 8 parity bits. Sixty-four write protect bits, each denoting 4096 words of memory, make possible write protection of any portion of a full size main store, 262,144 words. No test is made in the main store of the parity over the write protect register. Since the contents of the write protect register can be written or read via the main store bus, the integrity of the write protect register is tested when it is read back on the main store bus.

4.03 Loading the complete 72 bits of the write protect register requires four main store cycles, likewise four main store cycles are required to read the full contents of the register via the main store bus. The contents of the write protect register is written or read from the main store data register, using the first 16 bits of the data register and the 2 data parity bits. The portion of the write protect register that is written or read is controlled by address bits 15, 16, and 17, symbol No. 1, and requires the proper address bits 18 and 19 to select the main store. Segment decoding symbol No. 2 is not using during reading or writing the write protect register, but is used to determine a write protect violation during a normal write cycle.

4.04 Two conditions can disable the operation of the write protect

register during write cycles. If a complement write is attempted in a write protected area of the main store, the write signal to the memory will not be inhibited and the error B signal will not be put on the main store bus. The second condition is the blind write command which, to be a valid command, must be accompanied by a hardware backplane option in the main store. A blind write command overrides the write protected register and inhibits error B.

4.05 Composite diagram 2 shows the two possible memory modules in a main store and the associated data bits and addresses used to write or read the contents of the write protect register. In two main store cycles, one complete memory module can be set to its write protected condition.

4.06 Composite diagram 3 is an abbreviated diagram of the circuitry for testing a normal write command, to ascertain if it is in a write protected area. The 64 flip-flops of the write protect register are shown in symbols 4 through 11. Each group of eight flip-flops is selected by the segment decoder, symbol No. 2, using address bits 12, 13, and 14. The individual flip-flop in each segment is selected by the module decoder, symbol No. 1, using address bits 15, 16, and 17. Utilizing six address bits in a 1-out-of-64 selection, the single flip-flop denoting 4096 words of memory is selected. If the selected flip-flop corresponding to the address is set, a write protect error will occur during a main store write cycle. The gated outputs from the write protect registers are all ORed on net T1NWP0.

4.07 Composite diagram 4 is a slightly different configuration of the write protect register and is drawn to illustrate the circuitry used to write the write protect register. Here, only four of the address select lines are needed to select two flip-flops in each symbol. When two of the flip-flops are selected by using the address bits 15, 16, and 17 and the decoded command, the data bus content is loaded into the flip-flops.

4.08 In a manner similar to composite diagram 4, the process of reading the write protect register is shown in composite diagram 5. The address links select two for the eight flip-flops in each symbol and, together with the decoded command for reading the register, the contents of 16 of the flip-flops are put on the data bus.

5. ERROR DETECTION (FS 5)

5.01 The error detection portion of the main store covers basically all the self-checking circuitry that is built into the main store for both diagnostic program control and cycle-by-cycle testing during normal operation. Most of the circuitry in FS 5 falls into three categories of error detection:

- (a) ERROR A - Hardware failure
- (b) ERROR B - Write protect error occurring during a write cycle
- (c) ERROR C - Data parity error occurring during a read cycle.

5.02 The quantity of circuitry involved in the self-checking features, which detect failures that produce error A, is considerably larger than the other categories. Since the three categories listed are somewhat independent, they will be dealt with as three separate items and any commonality between them will be covered.

5.03 The source of an error A signal on the main store bus is the error register, which is 16 bits in length. Presently only 13 of the 16 bits in the register are used. The error register is bit-sliced with each FA1060 CP containing 2 bits of the register. The outputs of each stage of the error register are ORed at net TERRORO, and a bit being set in any one of the stages will cause an error A on the main store bus. Composite diagram 1 is an overview of the error register showing an expanded view of one of the stages. There are three ways of setting a bit in the error register, but two of the ways are used only under program diagnostic control and will be discussed later. The normal input to the error register, terminal modifier ERINOIO, is the input from the self-checking circuitry that is active during normal store cycles. As mentioned previously, there are two stages of the error register on each bit-slice CP. The companion input to terminal modifier ERINOIO is input ERINLIO. The additional error register bits on bit-slice boards in a wide store, 26-bit words, are not used or connected.

5.04 The error A output on the main store bus does not define which individual or multiple bits are set in the error register. Under program control using the circuitry in FS 6, diagnostic access, the contents of the error register can be read by means of the main store serial I/O channel. The parity bits covering the error register contents are generated in FS 6.

5.05 Composite diagram 2 is a listing of the inputs to the error register including the inputs for the three sources of data that can be loaded. For this section, only the error load is considered, since the other two methods require the circuitry in FS 6 to initiate their loading.

5.06 The interconnection of circuit packs and FSs comprising each single error bit may be somewhat difficult to follow. For that reason, composite diagrams 3 through 15 show a breakdown of the circuitry for the error bits and any associated FSs. Along with each error bit composite is a short explanation of its

function. In some cases where the duplication of the circuitry would not give an adequate explanation of the operation of a gate or flip-flop, it is replaced by a written description of its purpose.

5.07 An important consideration in the communication with the main store is the control of the signal that is returned on the main store bus indicating a cycle completion. The two signals that mark the completion of a cycle are store complete and error C. The circuitry that reacts to main store data parity errors in both normal cycles and error correction cycles is shown in composite diagram 16. The response from the main store to data parity errors under various conditions follows:

Write cycle with no data parity errors	Return store complete
Write cycle with single or double parity error	Return store complete and error A (sets error bits)
Write cycle (complement write)	Return store complete (inhibit data parity test)
Read cycle with no data parity errors	Return store complete
Read cycle with single or double parity error	Return error C
Read cycle in automatic correction mode and single parity error	Return error C
Read cycle in automatic correction mode and double parity error	Return store complete (delayed until bit 13 time).

5.08 In composite diagram 16, the parity check circuitry for testing the contents of the data register is shown as symbols 2 and 3. During a write or a blind write cycle, net WTR0 is active, enabling a test of the data parity shown in symbol 4. A failure to have correct parity causes an error in the error register corresponding to the parity high or parity low data fields.

5.09 The remainder of the circuitry shown in composite diagram 16 deals with the control of the main store responses relative to data parity tests and automatic correction during read cycles. The results of the data parity tests, nets PHER0 and PLER0 are connected to both symbols 1 and 4. In symbol 1 the timing is generated for the store complete and the error C signals. The bit 13 time flip-flop is only set when a data parity failure occurs and provides the timing for the error C signal or the store complete signal during automatic correction cycles.

5.10 The normal signal path for generating an error C signal is via collector

tie TPER0 which will produce the error C output on net SERC00 when net FNSER01 goes active. The other collector tie TPER01 is only active during an automatic correction cycle and inhibits error C if a double parity error occurs. In symbol No. 1, during an automatic correction cycle, the output of the SCM flip-flop is inhibited if a parity error occurs. If the parity error is over both data fields, the store complete signal net SCW00 is enabled again and goes active when the bit 13 time flip-flop is set. The bit 13 time flip-flop provides the timing via gate ENSCMTM0 for the store complete signal in automatic correction cycles when a double parity error occurs.

5.11 The serial channel access to the main store is basically used for diagnostic and maintenance purposes. In addition, it is used to initialize the main store after a power-on or problem condition. The serial message, excluding parity and start code, contains 16 bits which are further subdivided into two 8-bit fields. One of the 8-bit fields is used directly to set up conditions in the main store and is designated by name as option bits. The other 8-bit field is encoded in a 4-out-of-8 code. A more detailed explanation of the serial message is covered in FS 6.

5.12 With regard to testing the 4-out-of-8 code combination, the philosophy in testing the integrity of the decoding is to pretest the circuitry by trying all possible combinations, then declaring the circuitry functional. After the initial tests to determine circuitry functions, the 4-out-of-8 code combination is used without further tests for failures.

5.13 Composite diagram 17 is an abstract of the circuitry for testing the 4-out-of-8 codes. Mathematically there are 70 possible combinations of the codes, but only 30 are used in the main store. After decoding the 4-out-of-8 code from the serial channel to 1 of 30 outputs, the 1 of 30 outputs is recoded to the original 4-out-of-8 code. The regenerated 4-out-of-8 code is then tested to determine that only 1 of 30 outputs from the decoded buffer register was active. If a failure in the chain exists, net IODECC0 is active. A failure condition in the 4-out-of-8 code testing will set a bit in the main store error register. Loading the error register is under control of the serial channel and is not the normal method of setting a bit in the error register, due to a failure in the self-checking circuitry in the main store. Buffer register bit 13, one of the option bits, enables the error register to be loaded with the results of the 4-out-of-8 code check. This is gated by net IOREST0, which is active after the completion of a serial channel message.

5.14 A write protect error occurs whenever a write cycle is attempted in an area of the main store designated as write-protected by the write protect register in

FS 4. When a write protect error is detected, the ERB flip-flop on the FA1065 CP is set and the error B signal is returned to the 3A CC. Net TINWF0 goes active when a write protect violation occurs, and if the main store cycle is a write, the ERB flip-flop is set. The blind write command is used in conjunction with a backplane wiring option that allows write cycles at any location in the main store regardless of the state of the write protect register. During a blind write cycle in a write protected area of the main store, the ERB flip-flop is inhibited from being set and no error B signal is returned to the 3A CC.

6. DIAGNOSTIC ACCESS (FS 6)

6.01 The diagnostic access portion of the main store is the principal means of exercising and testing the main store via the software diagnostic programs. All the diagnostic access is initiated from the serial I/O channel to control or set up conditions that will lead to finding problems or verifying the proper working order of the main store. As part of the main store diagnostic program, all facilities of the main store, address, data, and command buses are used, but in general the serial I/O channel is the means of setting up a condition which may be verified by another portion of the main store.

6.02 A transmission to the main store of a serial I/O message consists of 21 bits. Three of the bits are the start code, which signals when the full transmission is complete. Two of the bits are parity bits over two 8-bit data fields. The remaining 16 bits constitute the data field used to control the activities in the main store. The 16-bit data field is further subdivided into two 8-bit fields. The first of the 8-bit fields contains option bits which are used singly to set up eight separate or different conditions. The second 8-bit field is coded in a 4-out-of-8 code and is decoded to 1-out-of-30 outputs.

6.03 A full cycle of receiving a serial I/O message or transmission consists of receiving the full 21-bit message and retransmitting that message on the return channel with a different start code. The retransmission of the message is true with one exception - when one 4-out-of-8 code, E4, is received. The code E4 directs the main store to return the contents of the error register rather than the message received.

6.04 Composite diagram 1 is an overall view of FS 6, showing the serial I/O channel control in symbol 1 and the registers that are loaded with the I/O message in symbol 2. Shown as symbol 3 is the circuitry for decoding the 4-out-of-8 code and a parity generator for generating the parity bits covering the error register for the single command that returns the error register via the serial channel.

6.05 When a serial channel message or transmission is started, shift pulses generated in symbol 1 will shift the message into the 21-bit shift register. After the start code is detected by the circuitry in symbol 2, the shift pulses are inhibited, but the main store continues to receive a stream of all zeros data from the serial channel to use as timing for completing the cycle. After the start code is received in the shift register, the 16 data bits are loaded into the buffer register. The 16 bits now in the buffer register remain there until overwritten by another serial I/O transmission. Following the loading of the buffer register, the contents of the buffer register are reloaded into the 21-bit shift for transmission out of the main store, returning the original message in a loop-around fashion. Before the return transmission is started, a new start code is loaded into the shift register. The return message is then shifted out of the main store using the all-zeros bit stream which is still being received. The all-zeros bit stream which provides the timing for the return transmission, continues until the return message is received at its destination. There are no internal or external clocks to control the serial I/O channel in the main store. All the timing and shift pulses are developed from the actual bit stream, providing control for both receiving and retransmission of a serial message.

6.06 As mentioned previously, one command received from the serial I/O channel, E4, produces a return of the main store error register rather than a retransmission of the buffer register contents. When an E4 command is received, the timing that loads the buffer register back into the shift register is inhibited. Instead, the contents of the error register along with its parity check bits is loaded into the shift register for an outgoing transmission.

6.07 Messages that are received by the serial I/O channel and loaded into the buffer register remain there in a static condition and are not cleared until a new transmission is received. The static condition is true except for one option bit used to initialize a portion of the main store. That option bit is self-clearing and is covered in composite diagram 3.

6.08 While the main store can communicate with two serial I/O channels, there is a hierarchy that controls which channel is active and which channel has priority. In order for the main store to receive a serial transmission on channel 1, the SMSIO lead on the main store bus must go active. Lead SMSIO does not have to stay active, since the "receive and transmit on channel 1" order is latched and saved by the circuitry in symbol 1. Channel 0 is the priority channel, and any transmission of data on channel 0 will lock out channel 1. After a transmission on channel 0, bus lead

SMSIO must go active to allow channel 1 to gain access.

6.09 A more detailed drawing of symbols 1 and 2 is shown in composite diagram 2. The translation of the shift register bits to the buffer register bits is shown in symbol 2.

6.10 The data into the shift register should contain an overall even parity. An extra register, labeled PAR, is connected to the shift register to verify correct parity over the 21 bits loaded into the shift register. Each time shift register stage SHB20 changes state, the PAR register is toggled to keep track of the data stream. Correct parity is verified when register PAR ends up in the correct state.

6.11 The method and circuitry for receiving and retransmitting the serial I/O message is somewhat different. In the process of receiving a serial message, the data enters shifter stage SHB20 and is shifted towards shifter stage SHB0. When shift register stages SHB2, SHB1, and SHB0 have the correct start code, the shifting is stopped and the contents of the shift register are eventually loaded into the buffer register. In contrast to receiving the message, the retransmission does not use shift register stage SHB0, but uses register DOB in symbol 1 as the first stage of the shift register. Register DOB is connected to shift register stage SHB1. Putting the first stage of the shift register on the same circuit pack as the remainder of the transmission circuitry eliminates some timing problems.

6.12 Composite diagram 3 sorts out the circuitry in the main store that is involved in initialization. There are three sources of initialization:

1. Turning power on
2. 4-out-of-8 code OF - (serial channel)
3. Option bit 0 - (serial channel)

6.13 Not all of these initialization sources perform the same function. The power-on and 4-out-of-8 code OF sources initialize circuitry in the main store and the refresh address register. Option bit 0 also initializes the circuitry in the main store and, in addition, clears the write protect register. It does not clear the refresh address register.

6.14 There are a few restrictions and differences in the use of the various methods of initializing the main store. Option bit 0 is designed to be synchronous with the refresh cycles that are occurring, and the main store will prevent initialization until the completion of the refresh cycle. The 4-out-of-8 code, on the other hand, is not synchronous, and may destroy a portion of the memory. Therefore, the OF initialization should not

be used if the main store information must remain valid.

6.15 The option bits and the 4-out-of-8 codes result in forcing some point or points in the main store into an active state as part of the main store diagnostics. Each of the valid 4-out-of-8 codes and the option bits are listed in composite diagram 4 along with their function or action. The 4-out-of-8 codes are listed as their hexadecimal equivalent, with buffer register bit P11 being the most significant digit and B5 being the least significant digit. The option bits are listed relative to their location in the buffer register. In the use of the serial I/O channel there is a difference between how the 4-out-of-8 codes and how the option bits are loaded into the buffer register. Once an I/O order is loaded into the buffer register, it remains there until it is overwritten with another succeeding I/O order. When the option bits that are already in the buffer register are not changed from one I/O order to another, the outputs remain in a steady state because they are loaded into the buffer register using double rail inputs. In contrast, the 4-out-of-8 codes are loaded into the buffer register using clear and gate inputs and even if an output does not change state between two successive transmissions, the output of the buffer register may have glitches.

7. MEMORY (FS 7)

7.01 The memory portion of the main store is divided into modules that contain 131,072 words of memory. The number of bits in a word can be either 26 or 18. Both include 2 bits of parity check bits. The narrow word size is obtained by not inserting four memory planes, each containing 2 bits of the word. The memory modules are configured in a bit-slice arrangement with each memory plane containing 2 bits of the word. Composite diagram 2 shows the CP layout along with the bit assignments for each CP. Also shown on diagram 2 are the memory module assignments.

7.02 Except for the read and write data lines, all the memory planes in a memory module are driven in parallel from the fanout board. The read data lines and the write data lines are connected directly to the data registers in the main store controller. The remainder of the necessary leads to the memory planes are provided by the fanout board and include address, refresh, and clock (GRAS0 and GCAS0) signals.

7.03 The fanout board for each memory module contains buffers and drivers as well as the selection of the memory module that will be active for a particular main store address. The fanout board circuitry multiplexes 14 of the address bits it receives and generates a second clock pulse, GCAS0. The timing relationships between the clocks and the

address bits are shown on composite diagram 1. The decoding of that portion of the address that selects a unique memory module is done on the fanout board and is part of a backplane wiring option. A refresh signal from the controller overrides the module selection and forces both memory modules in the main store to be selected.

7.04 Composite diagram 1 also contains a timing diagram of the timing relationships between the signals into and out of the memory plane.

8. TERMINATIONS (FS 8)

8.01 The terminations provide two functions in the main store. First, they provide a termination for the signal-lead connections between the memory and the main store controller. The termination impedance is approximately 100 ohms, which reduces the reflection on the signal paths to improve the wavefront rise time. Second, the terminations provide the logic level conversions between the +5 volt logic used in the memory to the +3 volt logic used in the controller.

8.02 The terminations covered in FS 8 are for all signal paths between the memory and the controller. In a main store unit, the controller-to-memory terminations are located on the bottom of memory modules 0 and 1.

8.03 If a bus-termination resistor assembly were missing, the main store could function properly, but would be working in a very marginal condition. To prevent this condition, all resistor assemblies are interconnected by a loop-through lead that causes a fuse alarm if one is missing.

8.04 Composite diagram 1 shows the interconnection of the bus-termination resistor assemblies. Also shown is a circuit view of how the bus-termination resistors are connected.

9. MEMORY POWER (FS 9)

9.01 Semiconductor memories and their support circuitry require certain precautions to insure that catastrophic failures do not occur due to improper inputs, supply voltages, or power sequencing. The memory power supplies are subdivided such that the power is self-contained for each main store memory unit that contains two memory modules. There are two power supplies, the J87421A-2 L2, supplying +5 volts to the logic, and the J87422B, supplying +12 and -5 volts. Both are used exclusively by the memory device.

9.02 A number of factors require that during the power-on sequence the +5 volts precede the +12 volts, and that the +12 volts be removed if the +5 volts is not present or out of regulation. While the clock input to the memory device is a major concern, all of the other circuitry on the

memory plane should not be without +5 volts when +12 volts is present.

9.03 Two methods are used to insure that the +5 volt power supply is functioning properly. The J87422B power supply has a sense input that is fed from the J87421A-2, L2 power supply, and the +12, -5 volts will not turn on until the +5 volts is present. In addition, the power alarm (PA) output from the +5 volt power supply is connected to the FC262 CP and, if the power supply senses an out-of-range output voltage, a fuse alarm is generated by the FC262 CP. Then all power in the main store is removed. For all remaining power supplies in the main store a PA alarm does not remove power, but only lights the LED on the power supply and provides an indication on the PA lead that an out-of-limits condition exists.

9.04 The fuse alarm outputs from both the J87422B and J87421A-2, L2 supplies are connected together and a fuse alarm from either power supply causes the power to be removed from the entire main store. Power is applied to the memory unit in a sequence controlled outside the main store. Two relays, STA and STB, provide contact closure to control the start inputs to the power supplies. The STA relay operates first and turns on all the power supplies in the main store, except the J87422B +12 and -5 volt power supplies. Between 0.5 and 1.5 seconds later, the STB relay operates and, if all other power supplies are normal as sensed by the FC262 CP, the FC262 supplies the +24 volts to the start lead of the J87422B power supply.

10. CONTROLLER POWER (FS 10)

10.01 Power in the main store, because of the large numbers and sensitivity of the memory devices, has a considerable amount of power-monitoring circuitry beyond the power alarm and fuse alarms that are part of each individual power supply. All of the added power control and monitoring internal to the main store is aimed at one purpose, to insure that all the main store power is up before the J87422B +12 and -5 volts is applied to the memory. In addition, it is important that the J87422B power supply be turned off if certain problems develop with any of the other power supplies in the main store.

10.02 The +3 volt power to the main store controller logic is supplied by four J87389F power supplies, symbols 1 through 4. A reference of +12 volts is furnished to the main store from an external source, and this voltage is converted to a +3 volt reference by two FC21 CPs, symbols 5 and 6. These provide the reference voltage to the four J87389F power supplies. The FC21 CPs also provide the filtering to the output of the J87389F power supplies. The power output of the J87389F is controlled externally to the main store by the STA relay, which supplies +24 volts to the

START inputs and turns on the +3 volt power supplies.

10.03

A power alarm from any of the J87389F supplies does not remove power from the main store, but lights an LED on the individual power supply that is causing the power alarm. An external connection from the main store indicates a power alarm. A fuse alarm from any of the J87389F power supplies causes all power to be removed from the main store. The fuse alarm connection to the power control circuitry, external to the main store, causes the STA and STB relay to remove the START voltage to all power supplies.

10.04

A test of the power alarm circuitry in each +3 volt power supply is activated when the power alarm test (PAT) input is made active. The results of the PAT appear on output NPA of each power supply. The PAT is activated and monitored external to the main store.

10.05 The FC262 CP provides both monitoring and control of the power in the main store. Symbol 7 shows the portion of the FC262 that monitors each of the four +3 volt power supplies and the +5 volt power that is used for 959B termination shown in composite diagram 1 of FS 8. This +5 volt power used in the memory termination is supplied to the main store from an external source. The additional monitoring of the J87389F power supplies in the main store, beyond the fuse alarm connection already mentioned, offers protection if power is applied to the main store with a +3 volt power supply missing. The connection of the fuse alarm outputs is inoperative when a power supply is not inserted in the frame. If the output of any of the +3 volt power supplies or the +5 volt termination power is missing, the FC262 circuit causes a fuse alarm and prevents power in the memory from being sequenced.

10.06

Symbol 8 covers connection for the PAT in the main store. As covered in FS 9, a separate power alarm loop for the J87421A-2, L2 +5 volt power supplies is provided because a power alarm from these power supplies forces a fuse alarm to exist in the main store. In order to test the power-alarm loop in the main store, a relay on the FC262 CP interconnects the two power-alarm loops, to provide a test of the power-alarm circuitry for all the power supplies. The power-alarm loops are interconnected when lead OSPAT0 is active.

10.07

To insure that the main store, and in particular the memory, does not come up in a high-power state, a power-on initialize is provided. The initialize condition is held until the start lead of the J87422B goes active and applies power to the memory. Symbol 9 shows the initialize connections.

11. DOUBLE-STORE READ

11.01 Double-store read is a technique which will allow the 3A CC to access the off-line store if an error is detected on reading data from the on-line store.

11.02 The mechanism for this technique, within the MASC, is a check of data parity during a store-read data cycle.

11.03 If this data-parity check fails, the store complete signal is blocked and the store error C signal to the 3A CC is activated.

12. COMPLEMENT CORRECTION

12.01 When an error is detected in data during a store-read operation, complement correction will allow the 3A CC to complement and write this data word into the location of the original, erroneous data word. Methods are also incorporated to identify such complemented data words and uncomplement the data word before the information is presented to the 3A CC.

12.02 The philosophy behind this procedure is that, if a single hard-bit failure occurs within memory, this bit will seem stuck either permanently logical one or zero. A data-parity failure indicates that a datum of opposite logical value has been expected to be written in this failure-bit location. By complementing the entire data word, the failed bit location will then contain the correct, inverted logical value. This procedure assumes only one failure per any data word and a failure that will remain permanently logical one or zero.

12.03 The complement write is effected by detection of an erroneous data parity. This blocks the store-complete signal activation and returns store error C to the 3A CC. The processor must then activate the complement-write signal lead to the store-write operation. Activating the complement write blocks normal load to the data and address registers, thus preventing loss of information from the data and address registers. It also gates the complement of the data registers to memory. The cycle thus proceeds as a normal store-write operation. As the entire data word has been complemented, both the data parity bits are also inverted, ie, set as in an error situation.

12.04 The complement read is effected when the processor activates the store-automatic correction signal lead during a normal store-read operation. Upon detection of both data parity bits in error, store error C processing is blocked, and gating paths are set to complement the stored data word before this information is presented to the processor. The stored complemented data word will appear to the processor as a normal data word.

SECTION III - REFERENCE DATA1. WORKING LIMITS1.01 Voltage Ranges

-48 V (-52.5V to -42.75V)
+24 V (+20.75V to +26.25V)

1.02 Temperature Range

0° to 49°C

1.03 Relative Humidity Range

0.0 percent to 90 percent

2. FUNCTIONAL DESIGNATIONS

<u>Designation</u>	<u>Meaning</u>
IOSC	I/O Subchannel
MAS	Main Store
MASB	Main Store Bus
MASC	Main Store Controller
MASCM	Main Store Controller and Memory Unit
3A CC	3A Central Control Circuit

3. FUNCTIONS

3.01 The MASCM performs the following functions:

- (a) Provides a means of storage for 128K words or 256K words of program or data information for the 3A CC
- (b) Provides a control interface between the 3A CC and the memory modules of the MAS
- (c) Provides collection and transmission of diagnostic information from the MAS to the 3A CC, as well as diagnostic access to the MAS from the 3A CC.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

- (a) Processor Frame Circuit -SD-1C910-02.
- (b) Processor Frame Power Circuit -SD-1C911-02.
- (c) Supplementary Main Store Power Circuit -SD-1C914-01.
- (d) Supplementary Main Store Frame Circuit -SD-1C915-02.
- (e) Auxiliary 3A Processor Frame Circuit -SD-4C007-02.

5. MANUFACTURING TESTING REQUIREMENTS

Intermediate Requirements

5.01 Manufacturing testing requirements are specified in X-78890. When this circuit is used in the supplementary main store frame (J1C065B-1), test requirements are specified in X-79251.

End Requirements

5.02 This circuit should be tested to verify that it is wired in accordance with the schematic and wiring drawings, that the requirements of the circuit requirements table are met, and that the circuit is capable of performing all functions stated in this circuit description.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-MM-LEG

